REMARKS

Claims 1 – 3 and 5 – 30 remain in the application. Claims 20 – 30 are allowed. Claims 4 – 19 are objected to but are indicated to encompass patentable subject matter. Claims 1 – 3 are rejected. Claims 31 – 35 are canceled herein without prejudice. New claims 36 – 38 are added. Claim 4 is canceled and rewritten as new claim 36. Claims 5, 6, 9, 18 and 19 are amended herein. No new matter is added.

The specification is amended to include the patent number of the related issued patent. No new matter is added.

Claims 4 – 19 are objected to for depending from rejected base claim 1, but are indicated to be allowable if rewritten in independent form. Claim 4 is canceled and rewritten as new claim 36 and claims 5, 6, 9, 18 and 19 are amended to depend from claim 36. Accordingly, claims 36 and 5 – 19 are allowable. New claims 37 and 38 are supported by claims 2 and 3, depend from claim 36 and so, are also allowable. Reconsideration and withdrawal of the objection to claims 36 and 5 – 19 and allowance of claims 36 and 5 – 19, 37 and 38 is respectfully requested.

Claims 1 – 3 are rejected under 35 U.S.C. §§ 102(b) and 103(a) as being unpatentable over U.S. Patent No. 5,684,760 to Hunter, alone. The rejection is respectfully traversed.

Hunter teaches a circuit for measuring a time interval. *See, e.g.*, the Title, the Abstract and col. 2, lines 3 – 11. More specifically, Hunter teaches measuring the length of a pulse provided to the input of the control circuit 5. Col. 2, lines 2 – 8 ("An input pulse signal **the period of which represents a time interval to be measured** is applied by way of an input terminal 4 to a control circuit 5,"). Furthermore, since Hunter is measuring an "input pulse signal," as far as the applicants can tell, this is an aperiodic or random pulse. There is nothing in Hunter that indicates or suggests that this input pulse is a global clock. Further, if it were a global clock, then "the commencement or leading edge of" each global clock cycle "applies an enable logic signal level to the synchronizer circuit 3 and to an error detecting circuit 6, and applies the inverse of that enable logic

signal level to a set of latches 7 associated with respective stages of the ring oscillator 1." *Id*, lines 8 – 10.

While measuring each clock cycle has utility, that is not what Hunter teaches or suggests. Therefore, Hunter fails to teach "a local clock buffer receiving a global clock and providing a local clock;" and therefore, fails to teach the present invention as recited in claim 1. Reconsideration and withdrawal of the rejection of claim 1 under 35 U.S.C. §102(b) is respectfully requested.

Regarding the rejection of claim 2 over Hunter, Hunter specifically teaches that "the circuit arrangement comprises a ring oscillator 1 comprising ten stages … ." Col. 12, lines 63 – 64. Leaving aside, whether an even number of stages will oscillate, Hunter does not teach or suggest that ten 100 picosecond stages is 6 Hunter "input pulse" signals long, as recited by claim 2 ("at least 3 global clock cycles long"). Bearing in mind that the period for the frequency provided by a ring oscillator is twice the delay through a ring oscillator (each edge, highgoing and lowgoing has to traverse the oscillator in each half cycle), it is apparent from Figures 3A and B that the Hunter ring oscillator provides a signal 13 that is much shorter than the "input pulse signal," at least by an order of magnitude. Therefore, Hunter fails to teach or suggest the present invention as recited in claim 2.

Regarding the rejection of claim 3 over Hunter, Hunter teaches a "'coarse' value for the length of the time interval … is … available from the count registered by the counter 2, while a 'fine' value of a fraction of a ring oscillator period may be derived from the latches 7, … ." Col. 2, lines 15 – 20. There is nothing here or anywhere else in Hunter to teach or suggest comparing adjacent register 7 edges. Therefore, Hunter fails to teach or suggest the present invention as recited in claim 3.

Moreover, dependent claims include all of the differences with the references, as the claims from which they depend. MPEP §2143.03 ("If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)."). Therefore, Hunter fails to teach or suggest the present invention as recited in claims 2 and 3, which depend from

claim 1. Reconsideration and withdrawal of the rejection of claims 2 and 3 under 35 U.S.C. §103(a) is respectfully requested.

The applicants thank the Examiner for efforts, both past and present, in examining the application. Believing the application to be in condition for allowance for the reasons set forth above, the applicants respectfully request that the Examiner consider new claims 36 – 38, reconsider and withdraw the objection to claims 36 and 5 – 19, reconsider and withdraw the rejection of claims 1 – 3 under 35 U.S.C. §§102(b) and 103(a) and allow the application to issue.

Should the Examiner believe anything further may be required, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below for a telephonic or personal interview to discuss any other changes.

Please charge any deficiencies in fees and credit any overpayment of fees to IBM Corporation Deposit Account No. 50-0510 and advise us accordingly.

Respectfully Submitted,

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(Date)

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